Advantages of MAX 9000 & MAX 7000S Architectures

The Altera® MAX® 9000 and MAX 7000S device families offer high density and high performance at a low cost. Combined with Altera's MAX+PLUS® II development tools—the most complete development environment available—MAX devices provide the best design solution. The MAX 9000 and MAX 7000S device architectures provide the following advantages:

■ *Product-term flexibility*—MAX 9000 and MAX 7000S device registers have five dedicated inputs: preset, clear, clock, clock enable, and a fast input select signal. Thus, each MAX device macrocell offers a product-term clock enable. In contrast, some competing devices use gated clock enables, which can cause designs to have glitches on the output if the clock and enable signals are not synchronized. In addition, some competing devices do not provide a fast input select signal in each macrocell.

■ *Output enable emulation*—MAX 7000S devices provide an optional open-drain output for each I/O pin, enabling these devices to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by several Altera devices. MAX 7000S devices can also provide an additional wired-OR plane. Most competing devices cannot emulate as many output enables.

■ *Less overhead*—The MAX architecture does not contain a clock generator and has propagation delay (t_{pd}) times that are architecture independent. Clock generators can add additional overhead and lengthen the clock period due to the extra delay.

■ *MultiVolt™ I/O operation*—MAX 9000 and MAX 7000S devices can be set for either 3.3-V or 5.0-V I/O operation. In contrast, some competing devices offer only 3.3-V or 5.0-V I/O operation.

■ *Highly integrated development tools*—The MAX+PLUS II development system provides seamless integration with the MAX architecture, allowing designers to migrate existing designs to higher density devices. In contrast, competing vendors rely on third-party developers for development tools, which can prevent the software from cleanly supporting features in the target architecture.

Performance

Altera Applications recently compared the performance of the MAX 7000S architecture to the Vantis MACH5 architecture (Vantis is the new name for AMD's programmable logic subsidiary). MAX 7000S devices out-perform MACH5 devices when implementing synchronous and asynchronous registered logic, as shown in Tables 1 and 2.

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Table 1. MAX 7000S & MACH5 Synchronous Register Performance

Parameter	Performance (MHz)	
	M5-128 **−7 Speed Grade** *(1)*	**EPM7128S** **−7 Speed Grade** *(2)*
Maximum frequency (synchronous)	166.7	166.7
Maximum frequency (register feedback)	125	125
f_{MAX} (register 1 feedback from different block to register 2 input)	105	125
f_{MAX} (register 1 feedback from different segment to register 2 input)	77	125
Maximum frequency (I/O feedback)	100	100
f_{MAX} (I/O feedback from different block to register 2 input)	87	100
f_{MAX} (I/O feedback from different segment to register 2 input)	67	100

Table 2. MAX 7000S & MACH5 Asynchronous Register Performance

Parameter	Performance (MHz)	
	M5-128 **−7 Speed Grade** *(1)*	**EPM7128S** **−7 Speed Grade** *(2)*
Maximum frequency (synchronous)	125	125
Maximum frequency (register feedback)	83.3	125
f_{MAX} (register 1 feedback from different block to register 2 input)	74	125
f_{MAX} (register 1 feedback from different segment to register 2 input)	59	125
Maximum frequency (I/O feedback)	71	100
f_{MAX} (I/O feedback from different block to register 2 input)	64.5	100
f_{MAX} (I/O feedback from different segment to register 2 input)	52.6	100

Notes to tables:
(1)   Source: *The MACH5 Family Fifth Generation MACH Architecture*, March 1996, revision B.
(2)   Source: *MAX 7000 Programmable Logic Device Family Data Sheet*, June 1996, version 4.

The documents listed below provide more detailed information. Part numbers are in parentheses.

- *MAX 9000 Programmable Logic Device Family Data Sheet* (*A-DS-M9000-04*)
- *MAX 7000 Programmable Logic Device Family Data Sheet* (*A-DS-M7000-04*)

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